WE CLAIM:

1. A testing apparatus having probes to be brought into contact with electrodes of a semiconductor device as a test, comprising:

a plurality of beams supported by support portions of a substrate, wherein said probes are formed on said beams; and

first lines to connect said probes to secondary electrodes formed on said substrate and second lines to connect said beams to said support portions, wherein said first and second lines are formed on said beams.

2. A testing apparatus having probes to be brought into contact with electrodes of said semiconductor device as a test, comprising:

a plurality of double-support beams that are supported by support portions of a substrate, wherein said probes are formed on said beams; and

lines to connect said probes to secondary electrodes formed on said substrate;

wherein each said line is formed on one of said double-support beams and extends from both sides of one of said probes on a face of said beam where said probe is formed.

3. A testing apparatus having probes to be brought into contact with electrodes of said semiconductor device as a test, comprising:

a plurality of cantilevers supported by support portions of a substrate, wherein said probes are formed on said cantilevers; and

wiring lines to connect said probes to secondary electrodes formed on said substrate,

wherein each of said lines is formed on a front face and a back face of said cantilever where said probe is formed.

4. A testing means for testing a semiconductor device, comprising:

a plurality of cantilevers supported by support portions of a substrate;

contacting means formed on one side of said cantilevers for contacting with electrodes of said semiconductor device as a test subject;

electrical connecting means for connecting said contacting means to secondary electrodes formed on said substrate via a face of a base portion of said cantilevers; and

support means for strengthening the cantilevers during deformation of the cantilevers, said support means being formed on said one side of said cantilevers and extending at least at the base portion of the cantilevers.

5. A testing apparatus having probes to be brought into contact with electrodes of said semiconductor device as a test, comprising:

a plurality of cantilevers supported by support portions of a substrate, wherein said probes are formed on said cantilevers; and

wiring lines connecting said probes to secondary electrodes formed on said substrate via a back face of said probes of said cantilevers, wherein said wiring lines extend from said cantilevers to said support portions on a front face of said probes of said of cantilevers.

6. A testing apparatus for testing a semiconductor device, comprising:

a plurality of double-support beams supported by support portions of a silicon substrate;

probes that are projections formed on said beams and to be brought into contact with electrodes of said semiconductor device as a test subject; and

wiring lines that connect said probes to secondary electrodes formed on said silicon substrate, wherein said wiring lines are formed on a face of said double-support beam where said probes are formed, so as to extend to two support portions at both ends of said beam.

7. A testing apparatus for testing a semiconductor device, comprising:

a plurality of cantilevers that are supported by support portions of a silicon substrate;

probes that are projections formed on said cantilevers and to be brought into contact with electrodes of said semiconductor device as a test subject; and

wiring lines to connect said probes to secondary electrodes formed on said silicon substrate, wherein said wiring lines extend from a front face of said cantilever where said probe is formed to said secondary electrode via a back face of said cantilever, and extend at least to the support portion of the associated cantilever on said front face of said cantilever.

8. The testing apparatus according to claim 1;

wherein each said probe formed on one of said beams is distanced from and adjacent probe formed on an adjacent beam by 100 μm or less.

9. The testing apparatus according to claim 4;

said support means is comprised of said electrical connecting means.

10. A semiconductor device manufacturing method comprising;

a test process including at least one of a characteristics test process;

an initial defect accelerated selection test process; and

a final performance test process that are to be executed on LSIs formed on a wafer or individual LSIs obtained by cutting a wafer;

wherein said test process is executed by using a testing apparatus comprising,

a plurality of cantilevers supported by support portions of a substrate;

probes formed on said cantilevers and to be brought into contact with electrodes of said semiconductor device as a test subject; and

lines to connect said probes to electrodes formed on said silicon substrate, wherein said probes are located between said electrodes and end of said lines.

11. A semiconductor device manufacturing method comprising;

a test process including at least one of a characteristics test process;

an initial defect accelerated selection test process; and

a final performance test process that are to be executed on LSIs formed on a wafer or individual LSIs obtained by cutting a wafer;

wherein said test process is executed by using a testing apparatus comprising:

a plurality of double-support beams supported by support portions of a silicon substrate,

probes formed on said beams and to be brought into contact with electrodes of an LSI as a test subject,

wiring lines to connect the probes to secondary electrodes formed on said silicon substrate, wherein said wiring lines are formed on a face of said double-support beams where said probes are formed and extend to said two support portions at both ends of said beam.

12. A semiconductor device manufacturing method comprising;

a test process including at least one of a characteristics test process;

an initial defect accelerated selection test process; and

a final performance test process that are to be executed on LSIs formed on a wafer or individual LSIs obtained by cutting a wafer;

wherein said test process is executed by using a testing apparatus comprising,

a plurality of cantilevers supported by support portions of a silicon substrate;

probes formed on said cantilevers and to be brought into contact at a front face of said cantilevers with electrodes of said semiconductor device as a test subject,

lines to connect said probes to secondary electrodes formed on the silicon substrate via a back face of said cantilevers, wherein said lines extend from said cantilevers to said support portion on said front face of said cantilevers.

13. A testing apparatus having probes to be brought into contact with electrodes of said semiconductor device as a test, comprising:

a plurality of cantilevers supported by support portions of a substrate, wherein said probes are formed on a first surface of said cantilevers;

a wiring line to connect said probes to secondary electrodes formed on said silicon substrate wherein said wiring line extends along a second surface of said cantilevers opposite said first surface.

14. A testing apparatus according to claim 1, wherein said beams are double-support beams, said first lines are located on a first side of said probes, and said second lines are located on another side of said probes on a front face of said double-support beams.

15. A testing apparatus according to claim 1, wherein said beams are cantilevers, said first lines are located at least on a back face of said cantilevers, and said second lines are located on a front face of said cantilevers.

16. A test device to test a semiconductor device, comprising:

a plurality of cantilevers supported by support portions of a substrate;

contact members formed on one side of said cantilevers to contact with electrodes of said semiconductor device as a test subject;

electrical connectors to connect said contact members to secondary electrodes formed on said substrate via a face of a base portion of said cantilevers; and

a support member to strengthen the cantilevers during deformation of the cantilevers, said support member being formed on said one of said cantilevers and extending at least at the base portion of the cantilevers.